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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,654	12/31/2003	Robert B. Staszewski	TI-35744	1713

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EXAMINER	
FILE, ERIN M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
05/14/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/749,654	STASZEWSKI ET AL.	
	Examiner	Art Unit	
	Erin M. File	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/31/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4, 6, 9, 10, 14, 17, 18, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Ahn et al. (U.S. Pub. No. 2002/0080891).

Claim 1, Ahn discloses:

- a digital transmitter path that provides a signal from a digital input, the transmitter path including at least one digital predistorter-that predistorts the digital input to mitigate nonlinearities associated with a power amplifier (fig. 2, 100, 110, 140, [0017]-[0019]);
- a receiver path associated with the digital transmitter path (fig. 2, 150);
- a coupling element that provides the signal from the transmitter path to the receiver path (fig. 2, [0002] discloses transceiver system which includes coupling transmitter/receiver);

- a signal evaluator that determines values for at least one parameter associated with the digital predistorter based on the signal (HPA modeling unit 180, [0043]-[0045]).

Claim 4, Ahn further discloses the power amplifier comprising an internal power amplifier that is integrated into the integrated transceiver circuit (fig. 2, power amplifier 140 is within the transceiver circuit).

Claim 6, 14, Ahn further discloses the digital transmitter path comprising an amplitude modulated path that provides a supply to the internal power amplifier from a first digital input ([0007], lines 3-8), and a phase modulated path that provides a radio frequency input to the internal power amplifier from a second digital input ([0007], lines 3-8).

Claims 9, 17, Ahn further discloses the phase modulated path comprising a digital predistorter that adjusts the second digital input to mitigate nonlinearities associated with the power amplifier ([0007], lines 3-8).

Claims 10, 18, Ahn further discloses the amplitude modulated path comprising a digital predistorter that adjusts the first digital input to mitigate nonlinearities associated with the power amplifier ([0007], lines 3-8).

Claim 21, Ahn discloses:

- providing a first digital signal, containing amplitude information related to a desired analog signal, to a transmitter path ([0007], lines 3-8);
- providing a second digital signal, containing phase information related to the desired analog signal, to the transmitter path ([0007], lines 3-8);

- predistorting at least one of the first digital signal and the second digital signal in the digital domain according to at least one predistortion parameter (fig. 2, 100, 110, 140, [0017]-[0019]);
- generating an analog signal from the first digital signal and the second digital signal (fig. 2, 120);
- processing the analog signal at a receiver path associated with the transmitter path to determine values for the at least one predistortion parameter (HPA modeling unit 180, [0043]-[0045]).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 11, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (U.S. Pub. No. 2002/0080891) as applied to claims 1, 6, and 21 above, and further in view of Park et al. (U.S. Patent No. 6,373,902).

Claims 2, 11, Ahn fails to disclose the transmitter path comprising a gain normalization component that transfers the digital input from a normalized domain to a domain that is dependent on process, voltage, and temperature (PVT) variations, however, Park discloses a gain normalization component that transfers the digital input from a

normalized domain to a domain that is dependent on process, voltage, and temperature (PVT) variations (col. 3, lines 35-57 discusses voltage compensation, col. 4, line 57, col. 5, lines 7-22 discuss temperature variations). Because compensating for these variations are well known in the art for reducing error in the system, it would have been obvious to one skilled in the art at the time of invention to incorporate the PVT variation compensations as disclosed by Park into the invention of Ahn.

Claim 3, Ahn discloses the digital predistorter preceding the gain normalization component on the transmitter path, such that the digital predistorter predistorts the digital input in the normalized domain (predistorter 110 of fig 2 before normalization of [0062]).

Claim 22, Ahn fails to disclose converting the first digital signal and the second digital signal from associated normalized domains to process, voltage, and temperature (PVT) dependent domains, however, Park discloses converting the first digital signal and the second digital signal from associated normalized domains to process, voltage, and temperature (PVT) dependent domains (col. 3, lines 35-57 discusses voltage compensation, col. 4, line 57, col. 5, lines 7-22 discuss temperature variations). Because compensating for these variations are well known in the art for reducing error in the system, it would have been obvious to one skilled in the art at the time of invention to incorporate the PVT variation compensations as disclosed by Park into the invention of Ahn.

5. Claim 5, 20, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (U.S. Pub. No. 2002/0080891) as applied to claim 1, 4, 21 above, and further in view of Kee et al. (U.S. Patent No. 6,724,255).

Claim 5, Ahn fails to disclose the internal power amplifier comprises a Class E switching amplifier, however, Kee discloses a Class E switching amplifier (col. 1, lines 19-22) which he discloses has the benefit of eliminating causes of switching power dissipation (col. 3, lines 18-23). Because of this advantage it would have been obvious to one skilled in the art at the time of invention to employ the Class E switching amplifier as disclosed by Kee into the invention of Ahn.

Claim 20, 23, Ahn fails to disclose comprising adjusting the value of the first digital signal to switch an associated power amplifier from a linear mode of operation to a saturated mode of operation, however, the switching amplifier as disclosed by Kee in claim 5 above meets the limitations of switching from a linear to a saturated mode which he discloses has the benefit of eliminating causes of switching power dissipation (col. 3, lines 18-23). Because of this advantage it would have been obvious to one skilled in the art at the time of invention to employ the Class E switching amplifier as disclosed by Kee into the invention of Ahn.

6. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (U.S. Pub. No. 2002/0080891) as applied to claim 4 above, and further in view of Kim et al. (U.S. Patent No. 2002/0034260).

Claims 7, 15, although Ahn fails to disclose the phase modulated path comprising a digitally controlled oscillator, however, Kim discloses the phase modulated path comprising a digitally controlled oscillator (fig. 4, NCO element 47). Numerically, or digitally controlled oscillators are well known in the art for their advantage of synthesizing a very wide range of precise frequency ratios. Because of this advantage it would have been obvious to one skilled in the art at the time of invention to employ the oscillator as disclosed by Kim into the invention of Ahn.

7. Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (U.S. Pub. No. 2002/0080891) and Kim et al. (U.S. Patent No. 2002/0034260) as applied to claims 7 and 15 above, and further in view of Park et al. (U.S. Patent No. 6,373,902).

Claim 8, 16, 19, neither Ahn nor Kim disclose the phase modulated path comprising a gain normalization component that adjusts the second digital input for PVT variations associated with the oscillator, however, Park discloses the phase modulated path comprising a gain normalization component that adjusts the second digital input for PVT variations associated with the oscillator (col. 3, lines 35-57 discusses voltage compensation, col. 4, line 57, col. 5, lines 7-22 discuss temperature variations). Because compensating for these variations are well known in the art for reducing error in the system, it would have been obvious to one skilled in the art at the time of invention to incorporate the PVT variation compensations as disclosed by Park into the invention of Ahn.

8. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (U.S. Pub. No. 2002/0080891) as applied to claim 1 above, and further in view of Neitiniemi (U.S. Patent No. 6,711,388).

Claims 12, 13, Ahn fails to disclose the power amplifier comprising an external power amplifier that is external to the integrated transceiver circuit and the power amplifier further comprising an internal power amplifier, however, Neitiniemi discloses a circuit with both internal and external power amplifiers (fig. 4, 406, 408). Because Neitiniemi discloses that thiese dual amplifiers allow for the advantage of more accurate power control (col. 2, lines 51-67), it would have been obvious to one skilled in the art at the time of invention to incorporate the dual amplifiers as disclosed by Nietiniemi into the invention of Ahn.

9. Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (U.S. Pub. No. 2002/0080891) in view of Park et al. (U.S. Patent No. 6,373,902)

Claim 24, Ahn discloses

- means for producing a digital input;
- means for predistorting the digital input to mitigate nonlinear error associated with a power amplifier according to one or more predistortion parameters (fig. 2, 100, 110, 140, [0017]-[0019]);
- means for generating an analog signal from the digital input (fig. 2, 120);

- means for analyzing the analog signal to determine appropriate predistortion parameters for the means for predistorting (HPA modeling unit 180, [0043]-[0045]).

Ahn fails to disclose means for converting the digital input from a normalized domain to a process, voltage, and temperature (PVT) dependent domain, however, Park discloses means for converting the digital input from a normalized domain to a process, voltage, and temperature (PVT) dependent domain (col. 3, lines 35-57 discusses voltage compensation, col. 4, line 57, col. 5, lines 7-22 discuss temperature variations). Because compensating for these variations are well known in the art for reducing error in the system, it would have been obvious to one skilled in the art at the time of invention to incorporate the PVT variation compensations as disclosed by Park into the invention of Ahn.

Claim 25, Ahn further discloses the means for generating the analog signal comprising means for synthesizing a radio frequency signal from a digital input. (fig. 2, 105, 130).

Claim 26, Ahn further discloses the means for analyzing the analog signal including means for applying a direct current (DC) offset to the signal ([0041]).

Claim Objections

10. Claims 8, 11, 16, 19, are objected to because of the following informalities: The acronym PVT must be properly defined in a similar manner as in Claim 2. Appropriate correction is required.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is (571)272-6040. The examiner can normally be reached on M-F 1:00PM-9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571)272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Erin M. File

EMF

5/2/2007

David C. Payne

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER